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THE PLASMA STATISTICS COMPUTER ABOARD EXPLORER XXXIV

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DAVID H. SCHAEFER
JAMES W. SNIVELY, JR.

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COMPUTER ABOARD EXPLORER XXXIV

by

David H. Schaefer
James W. Snively, Jr.*
Goddard Space Flight Center
Greenbelt, Maryland

ABSTRACT

A computing device that calculates quantities related to the mean, variance, and mode of the distribution of plasma as a function of the azimuthal angle of the spin stabilized satellite is aboard Explorer XXXIV. The device uses a combination of integrated circuits and discrete components including tunnel diodes. Performing computations aboard the spacecraft and telemetering the results of the calculations allows about twenty times more data to be sent than if the collected histograms were directly transmitted.

*Mr. Snively is presently with Computer Science Center, University of Maryland, College Park, Maryland.

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THE PLASMA STATISTICS COMPUTER ABOARD EXPLORER XXXIV

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INTRODUCTION

The Plasma Experiment^{1, 2} on the Explorer XXXIV satellite provides fertile ground for on-board data processing. In this experiment, a large amount of data is being produced by the sensing element, much too much to be completely transmitted over the available telemetry. In order to fit the experiment's data into the telemetry system, a parameter extraction technique was evolved where parameters related to mean, variance, and mode are computed aboard the satellite.

The problem of not enough telemetry bits available faced by this experiment even in earth orbit is a problem that will become more severe and affect more experiments as spacecrafts venture to greater distances from the earth where very low transmission rates are mandatory.

The purpose of the on-board processor (the "Statistics Computer") is to efficiently represent the prime characteristics of data collected by the plasma detector during a full rotation about its axis of the spin stabilized spacecraft. Figure 1 shows the type of output expected from the plasma detector in interplanetary space, and also in the region of space between the magnetosphere and the solar shock wave. In interplanetary space all plasma is expected to arrive from the direction of the sun, while in the transition region the plasma is expected to be

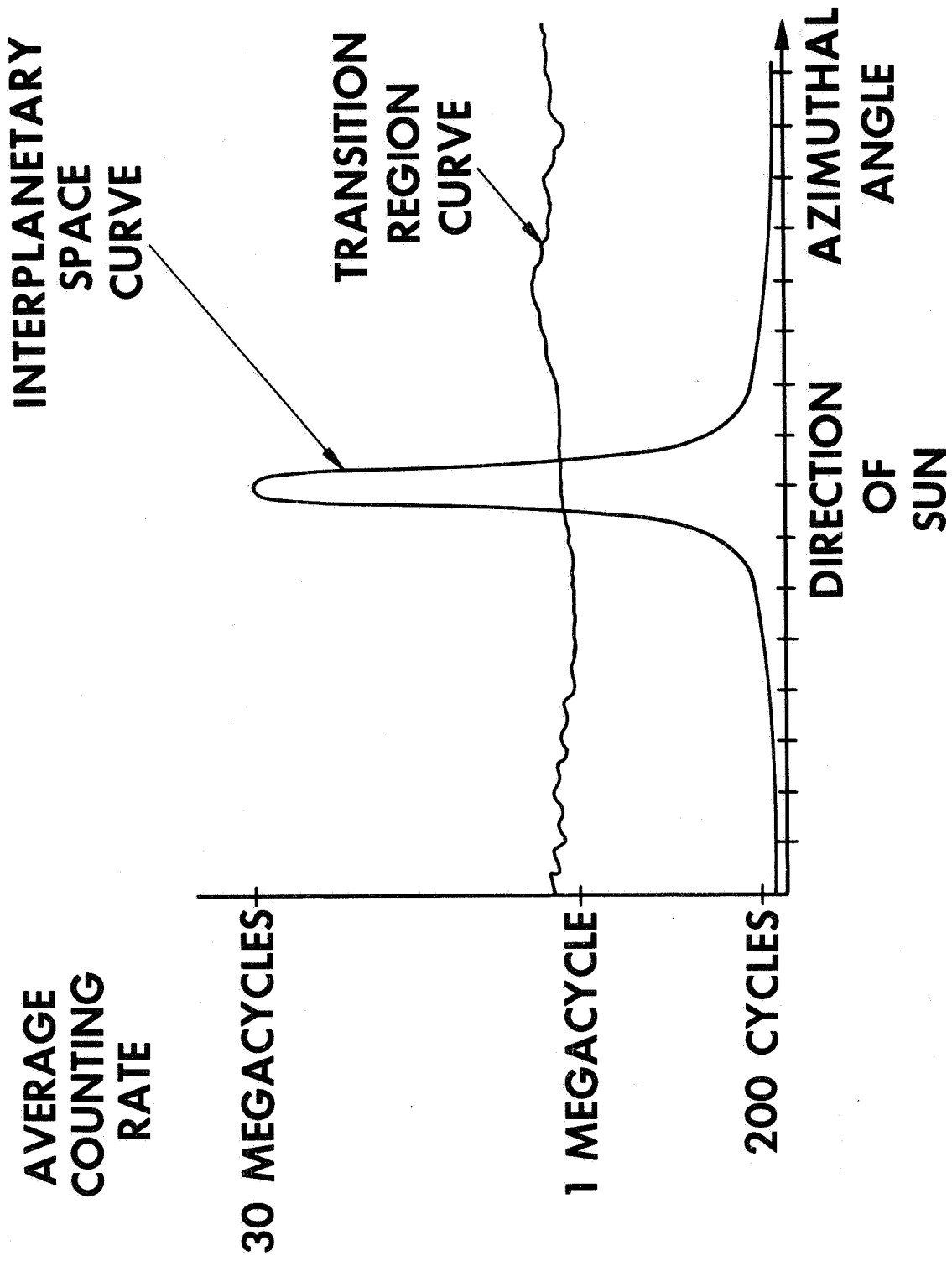


Figure 1—Typical input data.

homogeneously distributed. Questions of special interest are "Where is the boundary between the two regions?" and "How does the shape of an azimuthal angle versus counting rate curve change as the boundary is traversed?" In addition the usual questions of: "How much flux is present?" and "Where in each revolution was the counting rate the greatest?" ... need to be answered.

The process used to provide this information using a minimum number of bits is to calculate statistical quantities. Each revolution of the spacecraft about its spin axis is divided into 16 parts, each covering 22.5° of the revolution. Defining C_i as the number of pulses produced by the sensor in the i^{th} sixteenth of the revolution, we calculate a rough approximation to the quantity r as defined as

$$r = \frac{16 \sum_{i=1}^{16} C_i^2}{\left(\sum_{i=1}^{16} C_i \right)^2}$$

This quantity can only assume values between one and sixteen.³ If r has a value of 16 all inputs arrived in one-sixteenth of the revolution and the input curve is close to the interplanetary space input of Figure 1. On the other hand if the ratio r is 1, equal inputs arrived during every sixteenth of the revolution such as the transition region curve of Figure 1. Ratios in between 1 and 16 are indicative of various in between cases. Figure 2 indicates the shapes of histogram for various ratios. The bars of any histogram with the indicated ratio must lie within the shaded region shown.

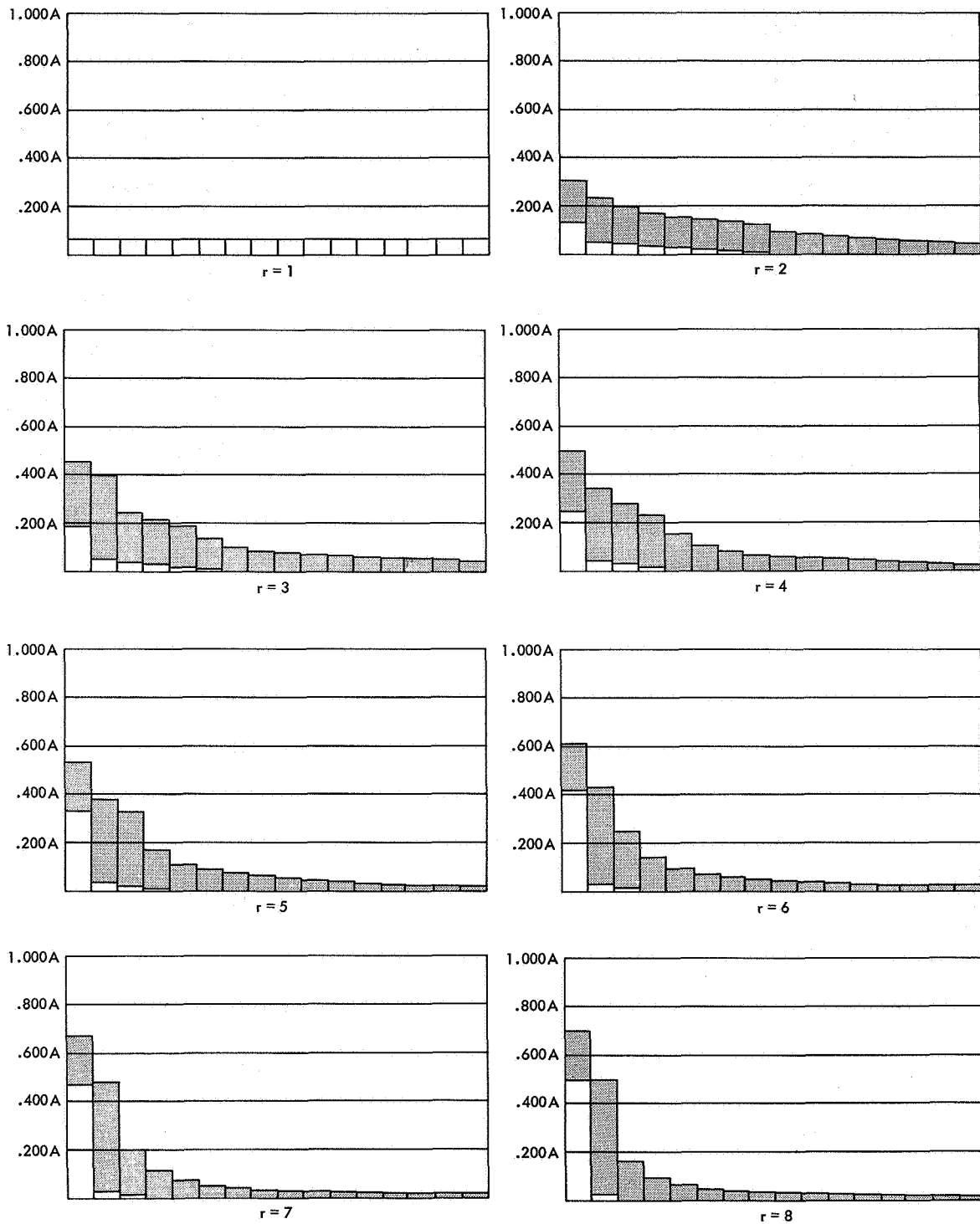


Figure 2 (1-8)—Longest and smallest bars for histograms with the indicated ratios. (The bars of any histogram with the indicated ratio must lie in the shaded region.)

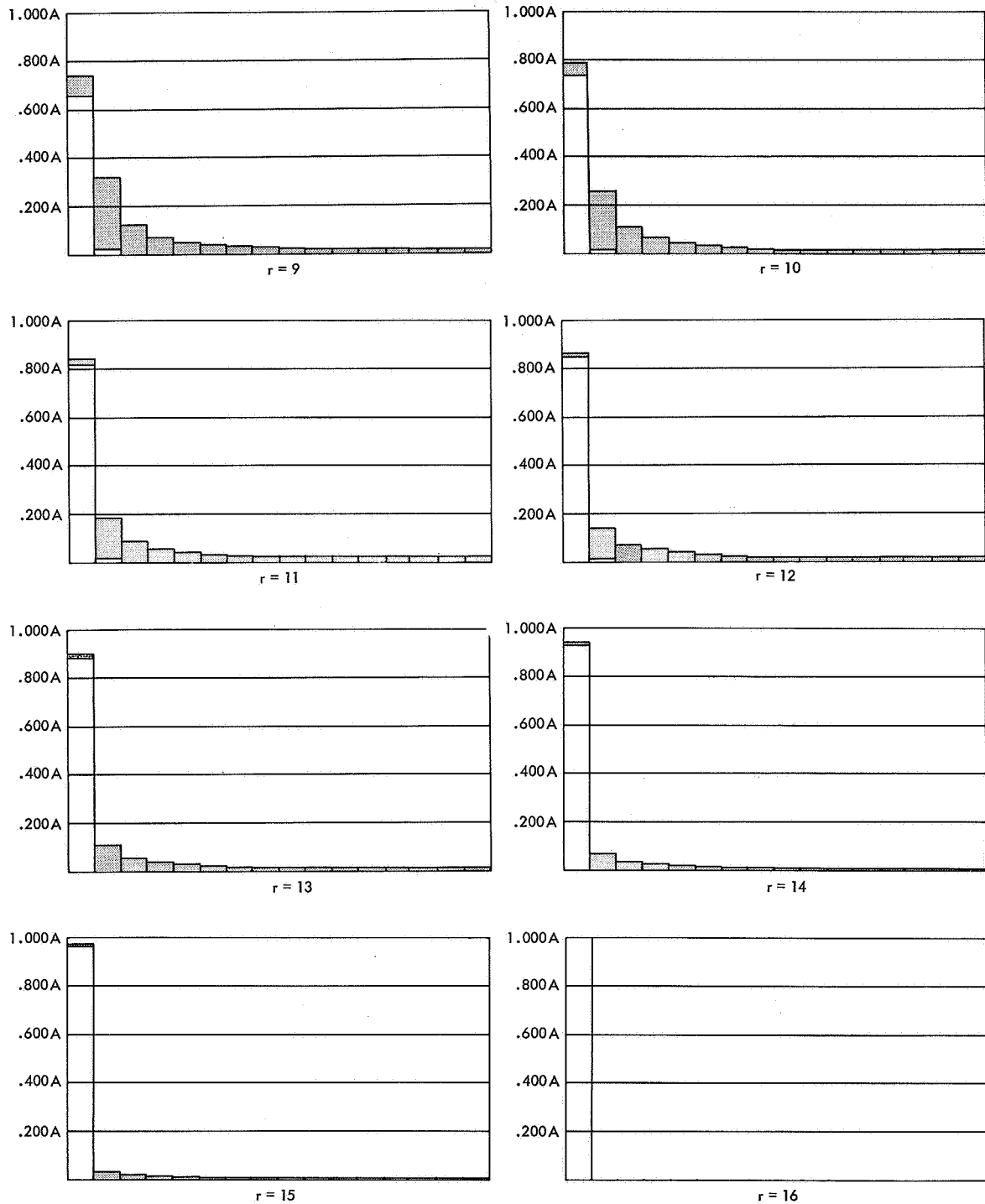


Figure 2 (9-16)—Longest and smallest bars for histograms with the indicated ratios. (The bars of any histogram with the indicated ratio must lie in the shaded region.)

To obtain the rough value of r the difficult operations of multiplication and division are not performed aboard the spacecraft. The sum of squares calculation is accomplished by a counting method. Four bits of this calculation are telemetered, these bits being determined by the logarithmic representation of the total number of counts received in the revolution, as shown in Figure 3. The logarithmic counter representation itself is also telemetered. From these quantities more refined values of r can be obtained on the ground.

It is possible to receive 2^{19} counts in any sixteenth of a rotation. To directly transmit the number of counts received in each sixteenth of a rotation over a complete rotation of the spacecraft would therefore require 16×19 or 304 bits. By doing the processing described in this paper a description of the information collected during a complete rotation of the spacecraft is represented by 16 bits, a bit saving of a factor of 19 over direct transmission of the data.

Figure 4 shows a segment of the output of a computer program that relates the output of the IMP flight hardware to the input data which produced the specified output. For example, if the logarithmic representation of the total number of pulses detected by the sensor (the A bits) is 195, the total number of counts actually detected lie between 38,912 counts and 40,959 counts. If, furthermore, the four transmitted bits of the squarer counter (the S bits) have the value 5, the ratio of the input histogram must be between 6.39 and 8.52. From this it can be calculated that the largest bar of this input histogram is between 17,048 counts and

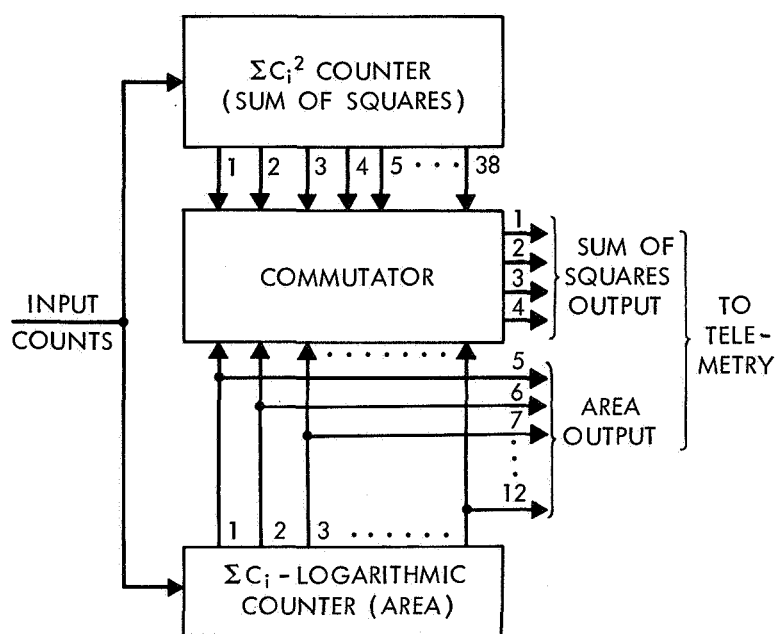


Figure 3—Block diagram of processor.

29,754 counts. For each of these quantities the harmonic mean (H.M.) of the range and the maximum \pm percentage error (P.E.) are also listed.

In addition to the above mentioned computations the Statistics Computer also provides an indication of which sixteenth of the revolution the number of received pulses was greatest.

The processor has many unique features. Although it is in essence a computer, it has no clock in the usual computer sense. Sequence of operations are determined by 1) the data itself, 2) inputs from an optical aspect system, and 3) the telemetry system which controls readout operations. Arithmetic operations are performed by the action of binary counters; this is an easy method of operating as the inputs to the device are pulses. Integrated circuits, conventional semi-conductors, and tunnel diodes are meshed in the device. The widespread use of tunnel diodes for shaping and triggering elements has been found particularly advantageous. In addition tunnel diodes are utilized in the ultra-high speed input counter that prescales the photomultiplier pulses.

LOGARITHMIC COUNTER

Logarithmic representation of the total number of counts received in a revolution is necessary as this number can vary over five orders of magnitude. A block diagram of the logarithmic counter is shown in Figure 5. This composite counter consists of two conventional counters. The first of these (counter A of Figure 5) counts the pulses generated by the photomultiplier after being counted down by a six-stage

LOGARITHMIC COUNTER

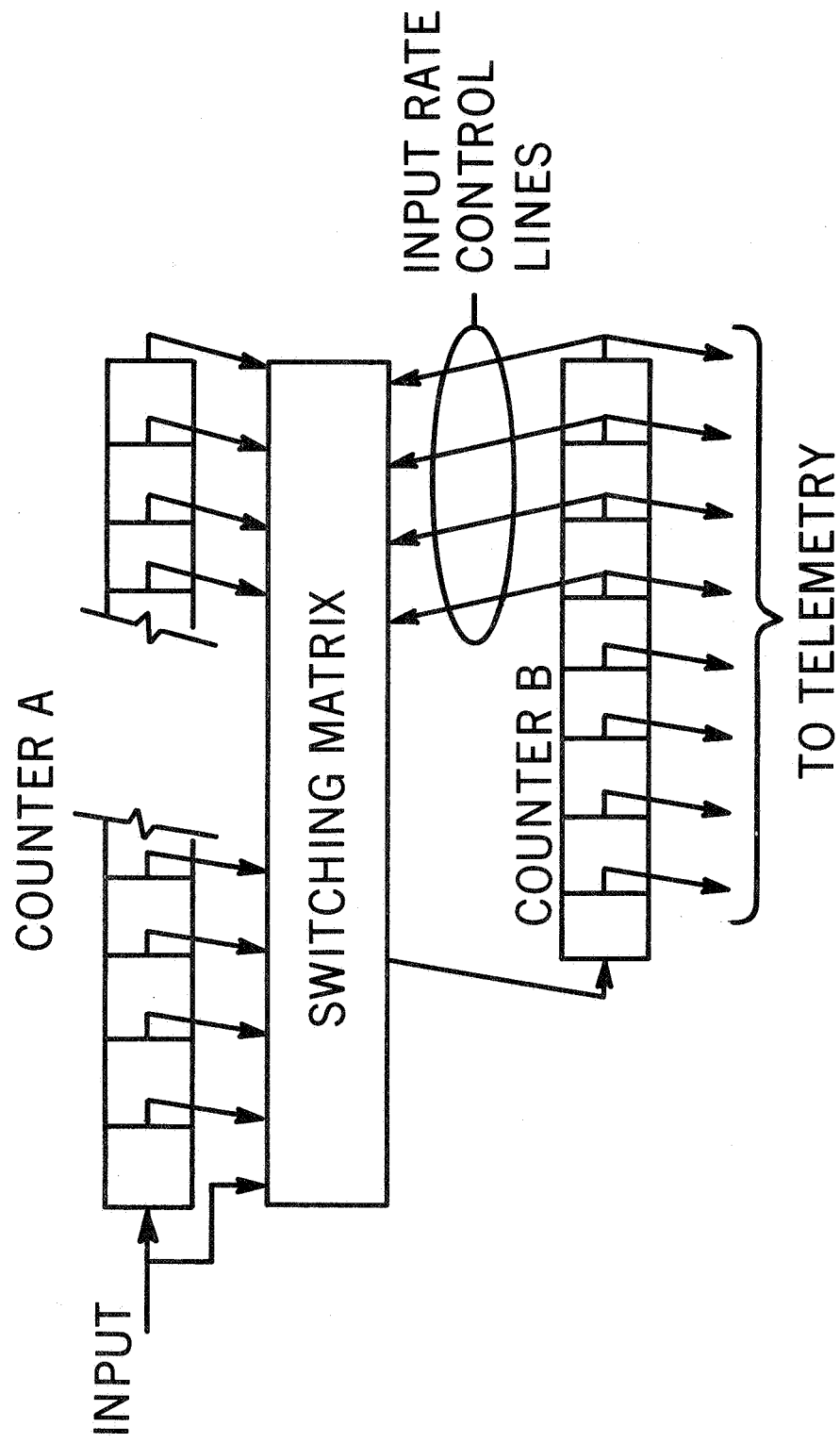


Figure 5-Logarithmic counter.

tunnel-diode counter affixed to the photomultiplier. The source of input pulses into counter B are controlled by the "input rate control lines" which come from the last four stages of counter B. Therefore this counter selects its own source of input pulses. In the beginning both counters are counting input pulses directly. After 32 counts arrive the matrix switches the input of counter B so that now its input is the output of the first stage of counter A. This means that counts come into counter B at one-half their previous rate. After 16 more counts are accepted by counter B (32 more by counter A) the input is again switched, this time the output of the 2nd stage of counter A being the input to counter B. After another 16 counts are accepted by counter B (64 more by counter A) the input is switched to the output of the third stage of counter A. This continues, every 16 counts into counter B reducing its input rate by two. The output from counter B therefore is roughly proportional to the logarithm of the number of input counts, the bigger the number in the counter, the more counts required to change it. A graph showing the relation between input counts and the output indication is shown in Figures 6 and 7.

SQUARING COUNTER

The rate of change of X^2 is proportional to X . It has long been known that the sum of odd numbers (i.e., $1+3+5+\dots+2n-1$) gives the square of n . The similar sum of integers (i.e., $1+2+3+\dots+n$) gives the value $n(n+1)/2$ which is within 6-2/3% of $n^2/2$ for n greater than 15, and this estimate improves as n gets larger. This latter is the relation used

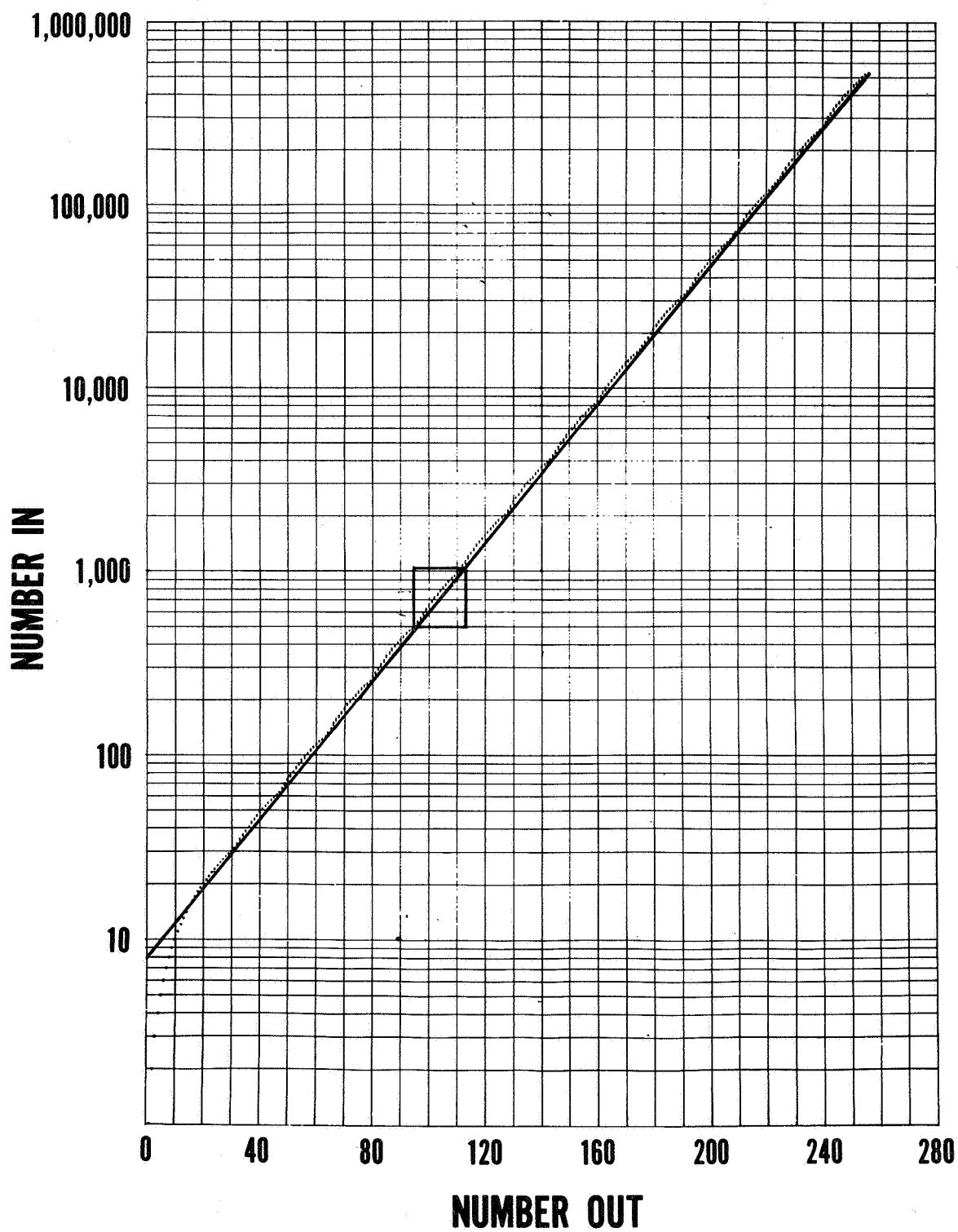


Figure 6—Output vs. input for 19 to 8 bit logarithmic counter.

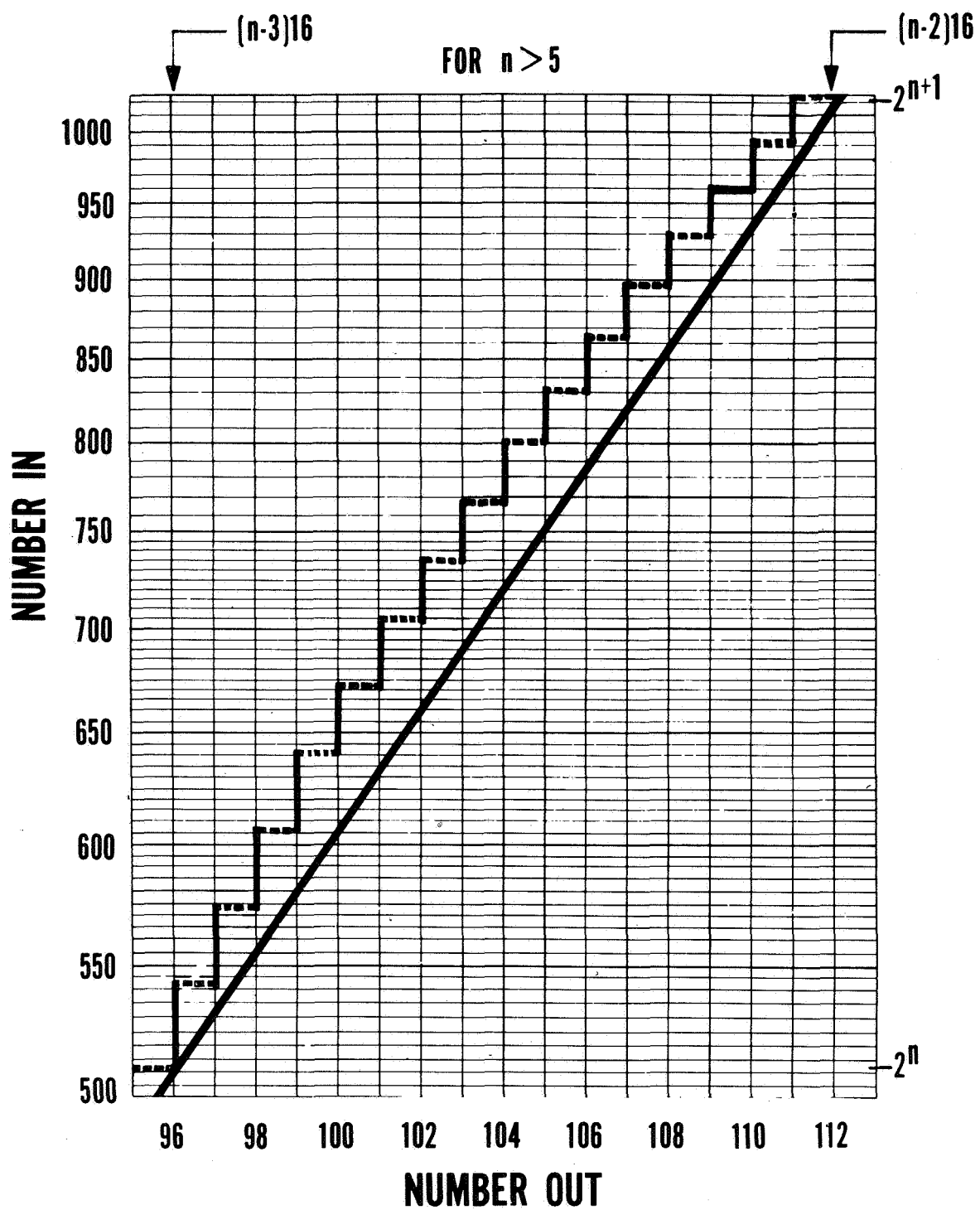


Figure 7—Detail of square shown in Figure 6. This figure can be generalized by use of the notation on the right and top of the figure.

for the squaring performed in the processor. A simplified version of the squaring counter is shown in Figure 8. Like the logarithmic counter, this counter is a composite containing two counters. Counter X is a standard counter. Counter Y is, however, unique in that it can receive input counts not only into its least significant stage, but also into stages above the least significant. A stage above the first one can receive counts from two sources—from the stage preceding it as in ordinary counters, and also from the outside. The D's in the figure are equivalent to one-shot multivibrators, each triggered by its predecessor thereby forming a delay chain. These delays are necessary to assure that two input pulses do not attempt to trigger a binary too close together. After a reset to zero the first input count puts a count into both counter X and, as the delay chain is activated by the count, also into counter Y. The second count changes the state of counter X to "2", therefore the action of the delay chain will deposit an input to only the second stage of counter Y. The third count will provide inputs to both stages 1 and 2 of counter Y. Therefore, as inputs are received counter Y is always incremented by the value of the number in counter X. In particular the series $1+2+3+\dots+n$ is presented to counter Y. At the end of each sixteenth of a revolution counter X is reset to zero while counter Y is not. Therefore at the end of a revolution of the satellite, counter Y contains a number closely proportional to the sum of squares.

In the actual data processor counter X consists of twelve stages while counter Y contains 27 stages. The input to the squaring portion of the data processor is from the fifth stage of counter A of the

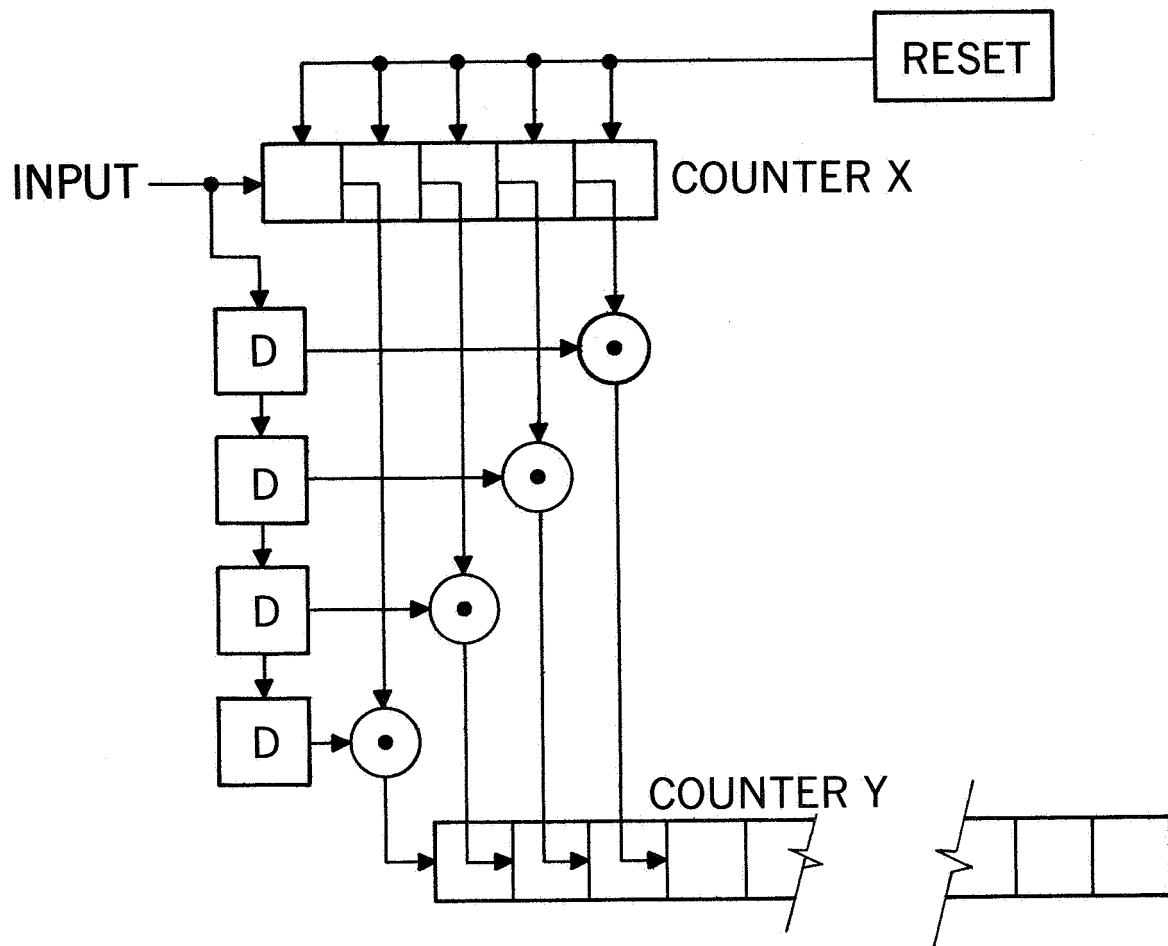


Figure 8—Squaring counter.

logarithmic counter. This relaxes the speed requirements of the squaring counter to one-thirty-second of that of the logarithmic counter. Resetting signals in synchronism with the spin rate are supplied by the optical aspect package which is part of the satellite central equipment.

SQUARER OUTPUT COMMUTATOR

After computing the sum of squares, it is necessary to provide a method of selecting four stages of the squaring counter for transmission. The four stages should ideally cover the four possible positions of the most significant bit of the number in the counter. In addition these four commutated stages must be uniquely determined from a reading of the logarithmic counter.

In practice these ideals have been closely approached. The scheme used for this four-bit commutation is schematically represented in Figure 9. The third stage of counter B of the logarithmic counter provides shifting pulses to a register that is initially storing a "one" in its 1st stage. The first shifting pulse is generated when 48 counts have been received by counter B of the logarithmic counter (which equals 64 actual counts having been received by the logarithmic counter as a whole). Every eight logarithmic count after this shifts the "one" one stage further. As these shifting pulses are generated by the logarithmic counts, the position of the "one" in the register is uniquely determined by the reading of the logarithmic counter. The "one" in the register is the actual commutating element. It activates gates that allow a given four bits of the squarer to reach the output shift registers.

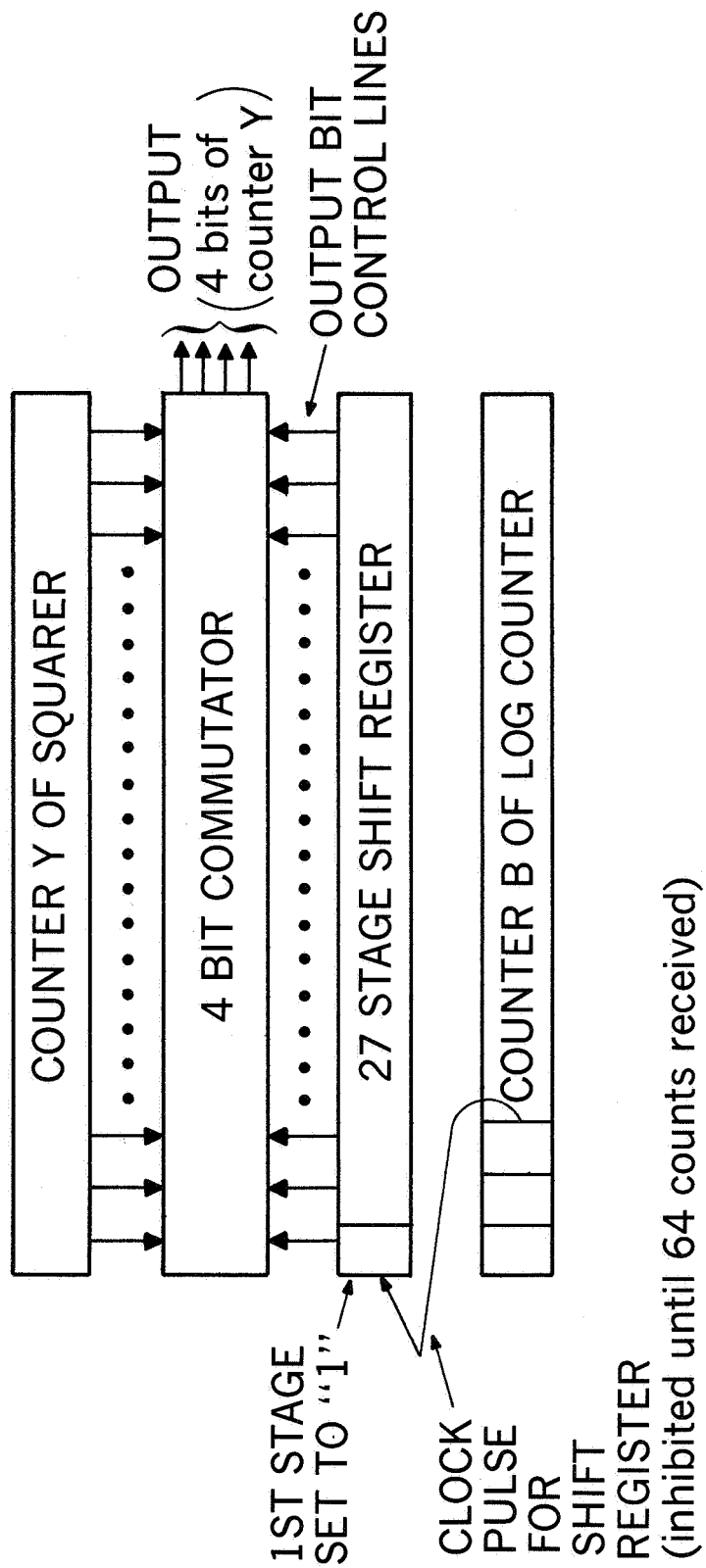


Figure 9—Squarer output circuitry.

Figure 10 is a plot of which stages of the squaring counter are read out for a given number of counts into the logarithmic counter. For example, if the logarithmic counter indicates that 30,000 counts have been recorded (a little less than 2^{15} counts), then Figure 10 shows that stages 16, 17, 18, and 19 of the squaring counter are being transmitted. At 2^{15} counts the squaring counter commutator shifts, and Figure 10 shows that for somewhat more than 2^{15} counts squarer stages 17, 18, 19, and 20 are transmitted.

The upper diagonal line of Figure 10 indicates the greatest value that the squaring counter can contain for any given number of input counts received by the logarithmic counter. The lower diagonal curve indicates the lowest value the squaring counter can contain under the same circumstances. The upper curve corresponds to the value that the squaring counter will contain for histograms with a ratio of sixteen while the lower curve corresponds to the values that this counter will contain for histograms with a ratio of one. To obtain numerical values for these curves the scale at the right hand side of the plot is used. It can be seen that there is good agreement between the possible locations of the most significant squarer bits, and the stages that are commutated.

MAXIMUM VALUE CIRCUITRY

At any time counter X of the squaring counter contains the number of counts received during the current interval. Therefore this counter along with a register can be used to determine whether the current interval has more or fewer counts than previous intervals.

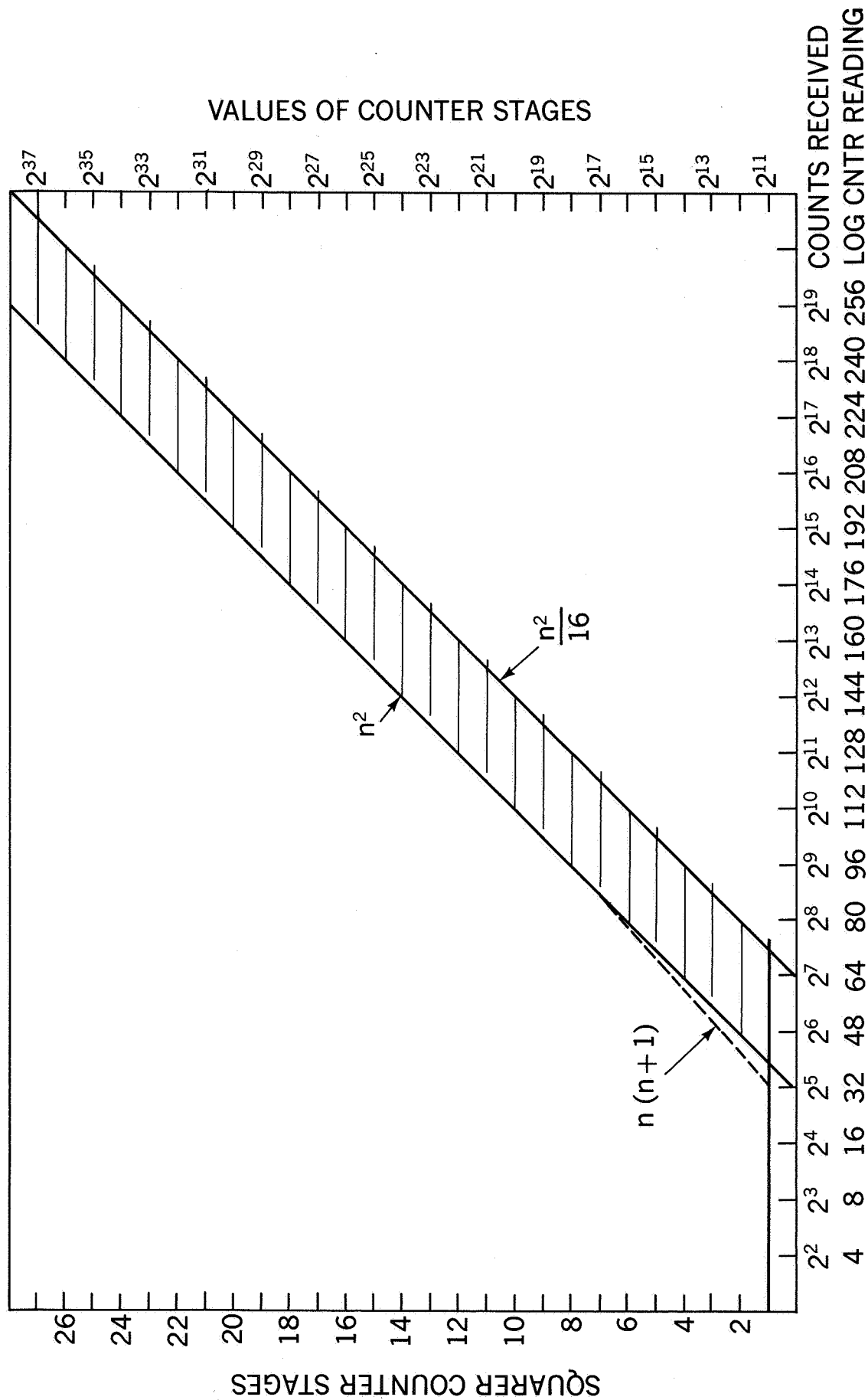


Figure 10—Squarer counter stages commutated vs. counts received.

The maximum value circuitry is straightforward. The counts received in the current interval are compared with a stored value in a register ("the maximum count register"), and if the current interval counts are larger than the stored number, this number is removed and replaced by the current count number. Whenever an updated number is stored in the maximum count register, an interval register is updated with the current interval number. A logic diagram of this circuitry is shown in Figure 11.

OUTPUT CIRCUITRY

During a spin of the satellite 16 bits of information are collected. The nominal spin rate is one revolution every 3 seconds. The length of time between telemetry readouts is 20 seconds. Therefore taking into account uncertainties as to when a complete spin will begin after the end of telemetry readout, and general uncertainties about spin rate, five revolutions worth of data can be collected for each data transmission. The 16 information bits describing a revolution are deposited in 16 four-bit shift registers at the end of the 1st four revolutions. The data from the fifth spin remains in the counters. At telemetry command the shift register's data is read to the encoder four bits at a time, by a combination of shifting and commutation. During this transmission period, data from the fifth spin sequences through the shift registers and on to telemetry. If for some reason the spin rate is much different from the nominal, the system will still operate. A very fast spin rate simply means that the data from five spins worth of data will be quickly

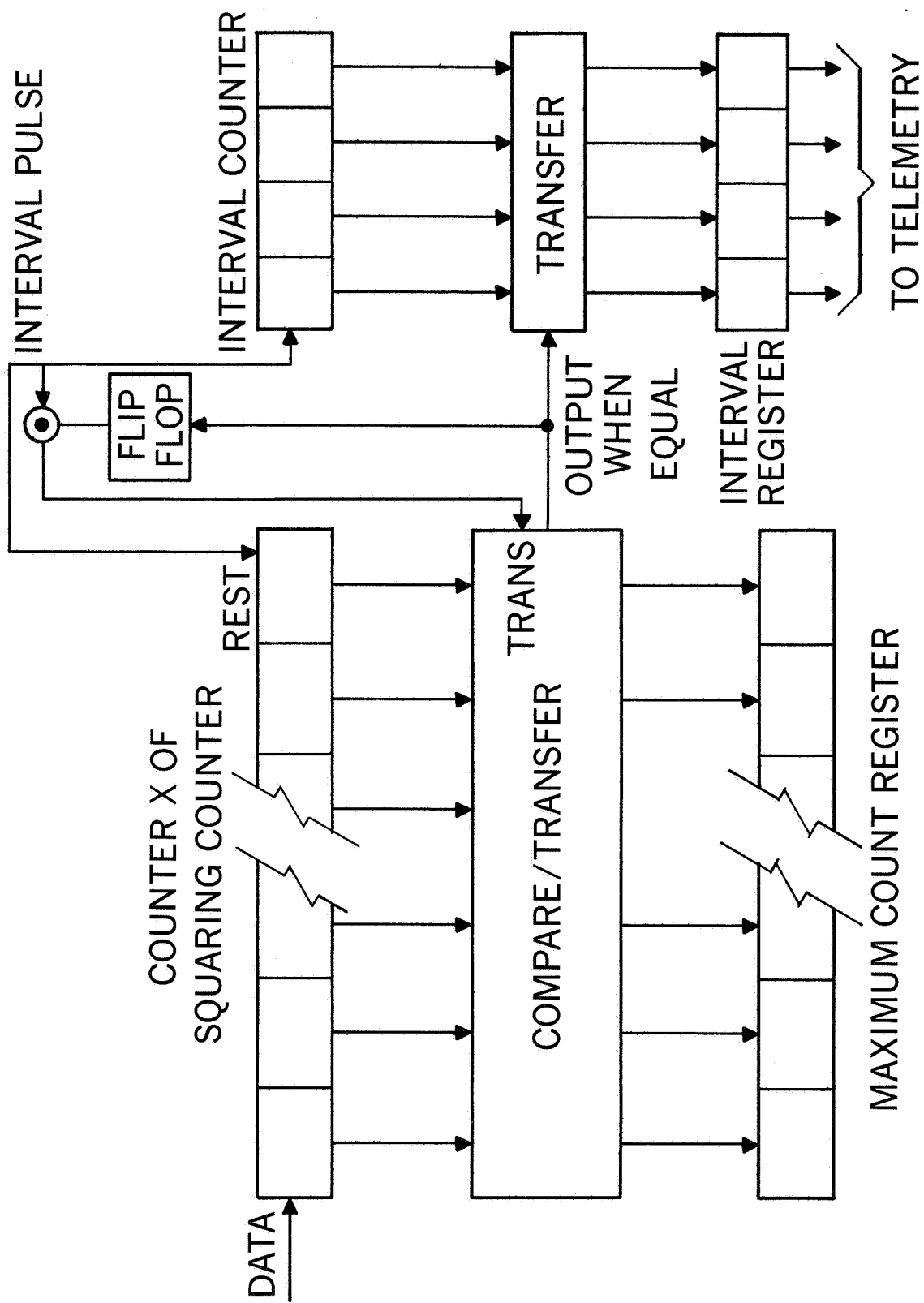


Figure 11 -Maximum value circuitry.

collected in the time interval immediately following telemetry. If, on the other hand, the spin rate is lower than expected, there may not be time for all five spins worth of data to be collected between transmissions. In this case the shift registers will still contain the information from the received spins, and this will be presented to telemetry.

TYPE OF COMPONENTS UTILIZED

The processor consists of 262 integrated circuits, sixteen tunnel diodes and a collection of discrete transistors, resistors, and capacitors. The integrated circuits are predominately of the series 51 Texas Instruments type.

The tunnel diodes are utilized as fast-rise-time triggers. They are the basic element in the squaring counter delay chain. They also play a prime role in pulse shaping inputs within the logarithmic counter.

The complete processor has been packaged in a standard IMP type module approximately $8'' \times 5'' \times 2''$. In order to pack all the circuitry into this space, multilayer board techniques were utilized. Figure 12 is a photograph of the processor before plotting. The power dissipation of the device is under 1 watt over the temperature range of -20°C to $+60^{\circ}\text{C}$.

ACKNOWLEDGMENT

The authors wish to give special mention to the late Edgar G. Bush, whose circuit developments made possible the realization of the Statistics Computer.

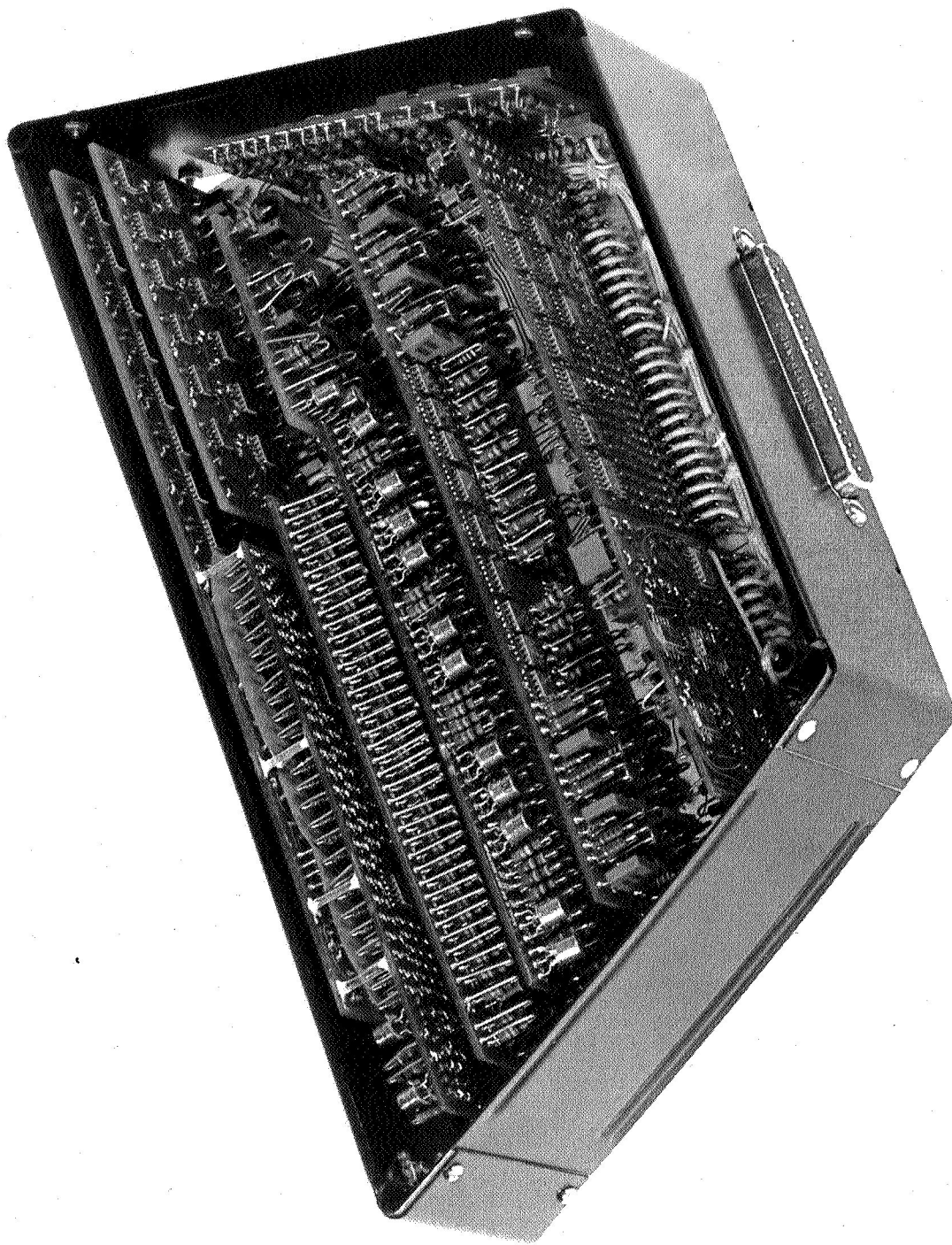


Figure 12—The complete package.

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- 1) The Crossed Field Velocity Selector, Ogilvie, Kittredge, Wilkerson, X-612-67-331.
- 2) A Mass Energy Spectrometer for Space Plasmas, Ogilvie, McIlwraith, Wilkerson, X-612-67-330.
- 3) A Statistical Data Compression Technique, James W. Snively, NASA TN D-3616.

APPENDIX

The Statistics Computer has been simulated on the APL terminal system using the programming language first defined by Iverson.*

The conversion of a number N into its logarithmic counter (CL) representation is as follows:

```

      ∇ L←CL N
[1]  MN←(19ρ2)⌈N
[2]  Z←(MN⌈1)⌊16
[3]  K←(4ρ2)⌈(16-Z)
[4]  J←Z⌊15
[5]  L←K,MN[(J+1),(J+2),(J+3),(J+4)]
      ∇

```

The output (line 5) represents the state of the binaries shown as Counter B in Figure 5.

The position of the "one" in the squarer output commutator shift register (the shift register of Figure 9) is a function of the logarithmic counter value exclusively. For an input vector C, the position of the "one" (the LAtch position) is

```

      ∇ B←LA C
[1]  B←(1+⌊((8α5)/(CL+/C)))⌈6
      ∇

```

where the initial position is assigned the value six.

The squarer (SQ) counter values are as follows for an input vector C (C is of dimension 16):

```

      ∇ S←SQ C
[1]  I←⌊(C÷32)
[2]  S←((27ρ2)⌈(+/(I×(I+1))÷2)), 1 1 1
      ∇

```

*See APL/360 - *The APL Terminal System: Instructions for Operation*. (Available from IBM, Watson Research Center, Yorktown Heights, New York).
Also - Iverson, Kenneth E., *A Programming Language*, Wiley, 1962.

The most significant 27 bits of the output, S, are the states of all the stages of the squaring counter (Counter Y of Figure 8). The trailing "ones" represent the value seen by the squarer output commutator when it "falls off" the least significant edge of the counter and is not commutating an actual squarer stage. This happens for small input values.

The value of the four commutated bits of the squaring counter (the "S Bits") are a function of the logarithmic counter (via the function LA) and the squarer (via the function SQ). These bits are defined as follows:

```

      ▽ G←SB C
[1]   B←LA C
[2]   S←SQ C
[3]   G←S[(33-B),(34-B),(35-B),(36-B)]
      ▽

```

The maximum value circuitry has as its input, counter X of the squaring counter. This counter is pulsed by every 32nd input pulse starting with the sixteenth. Taking these complications into account the value of the interval register at the end of a spin is given by the following function:

```

      ▽ A←MAX C
[1]   SV←[((SC C)+16)÷32)
[2]   N←115
[3]   DV←SV[1],SV[N+1]-SV[N]
[4]   A←16|((⌈/(((⌈/ DV)=DV)/116))
      ▽

```

The number of counts in counter X at the end of each interval is given by the vector DV.

The function SC above is the sum scan function that has not at the time of writing been implemented on the APL system. The following

function for sum scan has, therefore, been derived for vectors of dimension 16:

```

      ▽ SS←SC C
[1]   CS←C[1],+ /C[1 2]
[2]   N←3
[3]   CS←CS,+/ (CS[N-1],C[N])
[4]   N←N+1
[5]   →((N≠17)×3)+((N=17)×6)
[6]   SS←CS
      ▽

```

The actual telemetry format for data collected during one revolution of the satellite consists of four sixteen level pulse frequency modulation busts. The hexadecimal representation of this (the form of "quick look" data from the satellite) is given by the TELemetry function:

```

      ▽ P←TEL C
[1]   P←(1((8α4)/(CL+/C))), (1((8ω4)/(CL+/C))), (1SB C), MAX C
      ▽

```

All the foregoing specify the computer and its telemetered outputs.

A simple function useful in helping to reduce received data is the LG function. This function reduces the first two components of the telemetry vector to the approximate number of input counts. Its definition is:

```

      ▽ A←LG Y
[1]   →((Y[1]>1)×2)+((Y[1]≤1)×4)
[2]   A←1(1,((4ρ2)∓Y[2]),1,((Y[1]-2)ρ0))
[3]   →0
[4]   A←161Y
      ▽

```

Examples of the use of the TEL and LG functions follow. In the first three examples vector H has the ratio 16, vector E has the ratio 8,

and the vector ($16\rho 2440$) has the ratio 1. Figure 4 can be used in checking the answers for these three examples.

H
0 0 0 0 0 39040 0 0 0 0 0 0 0 0 0 0
TEL H
12 3 11 6
LG 12,3
39936
E
0 0 0 0 0 19500 19500 0 0 0 0 0 0 0 0 0
TEL E
12 3 5 7

TEL 16\rho 2440
12 3 0 14

A
1 2 300 400 500 600 70 800 90000 10 20000 12 13 14 15 16
TEL A
13 11 7 9
LG 13,11
112640
+/A
112753

TEL 2,15\rho 3
2 7 7 6
LG 2,7
47
TEL 16\rho 0
0 0 7 0